Notice of References Cited	Application/Control No. 10/811,410	Applicant(s)/Patent Under Reexamination KATAOKA, TOSHIHIKO	
	Examiner Faisal Zaman	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Nakashima et al., "An Accurate and Efficient Simulation-based Analysis for Worst Case Interruption Delay", 10/2006, ACM Press, Proceedings of the 2006 international conference on Compilers, architecture and synthesis for embedded systems, pages 2-12.
	V	Van der Wijngaart et al., "The Effect of Interrupts on Software Pipeline Execution on Message-Passing Architectures", 1/1996, ACM Press, Proceedings of the 10th international conference on Supercomputing, pages 189-196.
	W	Regehr et al., "Preventing Interrupt Overload", 6/2005, ACM Press, Proceedings of the 2005 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems, pages 50-58.
	X	De Gloria et al., "A Self Timed Interrupt Controller: A Case Study in Asychronous Micro-Architecture Design", 9/1994, IEEE, ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annual IEEE International, pages 296-299.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.